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[SYSTEM AND METHOD FOR IMPLEMENTING A MICRO-STEPPING DELAY CHAIN FOR A DELAY LOCKED LOOP]

Abstract

A delay locked loop for use in an integrated circuit device includes a coarse delay chain in series with a micro-stepped delay chain. The coarse delay chain includes a plurality of coarse delay units configured for selectively providing a coarse delay with respect to an input clock signal, and the micro-stepped delay chain is configured for selectively providing a fine delay adjustment with respect to the input clock signal. The micro-stepped delay chain further includes a plurality of parallel signal paths, wherein one or more of the parallel signal paths are capacitively loaded so as to provide the fine delay adjustment.